Chapter 49
Solutions for False Lock of FLL in GNSS Receiver

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Abstract The first stage of processing with a Global Navigation Satellite System (GNSS) receiver is signal acquisition process, while the second stage is Frequency Lock Loop (FLL) process. It was found that when sequentially adopting the "sliding correlation" acquisition strategy and the "dual-quadrant" frequency discrimination strategy, the FLL occasionally operates abnormally with hundreds Hz false lock error, while the sequential Phase Lock Loop (PLL) would steadily tracking but with incorrect output bit phase. Two simple and universal methods are proposed to solve above problem: A. Instead adopting the "four-quadrant" frequency discriminator; B. Inserting frequency false lock detecting and correction mechanism between "dual-quadrant" FLL and Phase Lock Loop (PLL). Theory analysis and simulation test show the validation of the solutions.

Keywords Global navigation satellite system (GNSS) · Frequency lock loop (FLL) · Frequency tracking discriminator · False lock

49.1 Introduction

The first stage of processing with a Global Navigation Satellite System (GNSS) receiver is signal acquisition process, while the second stage is Frequency Lock Loop (FLL) process. It was found that when sequentially adopting the "sliding correlation" acquisition strategy and the "dual-quadrant" frequency discrimination strategy, the FLL occasionally operates abnormally with hundreds Hz false lock error.

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As discussed in [1], the PLL could not detect and correct the frequency false lock phenomenon induced by FLL with "dual-quadrant" frequency discriminator. Taking GPS L1 C/A code as an example, under the condition of frequency false lock, the PLL can tracking steadily but with false and alternately-rolling predetection integration value, which result in the false recovered information bits. Base on above observation of alternately-rolling predetection integration value, a detecting and correcting mechanism for FLL frequency false lock problem was proposed in [1].

Limited application scope is the main drawback of [1] since it could NOT work for the situations of only one or two PRN code periods existing in one information bit (such as GALILEO E1-B), or the situations of high rate secondary code being modulated (such as GPS L5, GALILEO E1-C, E5a, and E5b).

To overcome the shortcoming of [1], two simple but universal solutions were proposed in this paper.

49.2 Mechanism Analysis for FLL Frequency False Lock Phenomenon

Well known by GNSS signal acquisition theory [2], the detection probability P_D is a function of predetection integration SNR C/N and acquisition threshold Th. For a given Th, P_D increases with C/N.

Predetection integration SNR is defined as $C/N = \beta\ (C/N_0)T_p$, where C/N_0 is the Carrier-to-Noise Ratio (Hz), T_p is the predetection integration time (s), β is the power loss caused by mismatch of PRN code phase and carrier frequency, which defined as

$$\beta = R_c^2(\varepsilon_{code})\frac{\sin^2(\pi f_d T_p)}{(\pi f_d T_p)^2} \tag{49.1}$$

where ε_{code} and f_d are the synchronization errors of PRN code phase (chips) and carrier frequency (Hz) respectively. Figure 49.1 gives the curve of β versus ε_{code} and f_d. Referring to Fig. 49.1, error patterns of <0.25 chips, 333.3 Hz> and <0 chips, 527.8 Hz> corresponding to the same power loss of $\beta = 0.38$.

Assuming the predetection integration time being $T_p = 1$ ms, the PRN code searching step during signal acquisition being $\Delta_{code} = 0.5$ chips, the carrier Doppler frequency searching step being $\Delta_{freq} = 2/(3T_p) = 667$ Hz. Generally speaking, conservation design expects the error pattern of $<\Delta_{code}/2,\ \Delta_{freq}/2>$ (i.e., <0.25 chips, 333.3 Hz>) being success acquired, resulting in β corresponding to designed acquisition threshold Th being lower than 0.38. Under such acquisition threshold, some error patterns with residual carrier Doppler frequency larger than $1/(2T_p) = 500$ Hz (such as <0 chips, 527.8 Hz>) could be false judged as "success acquisition".

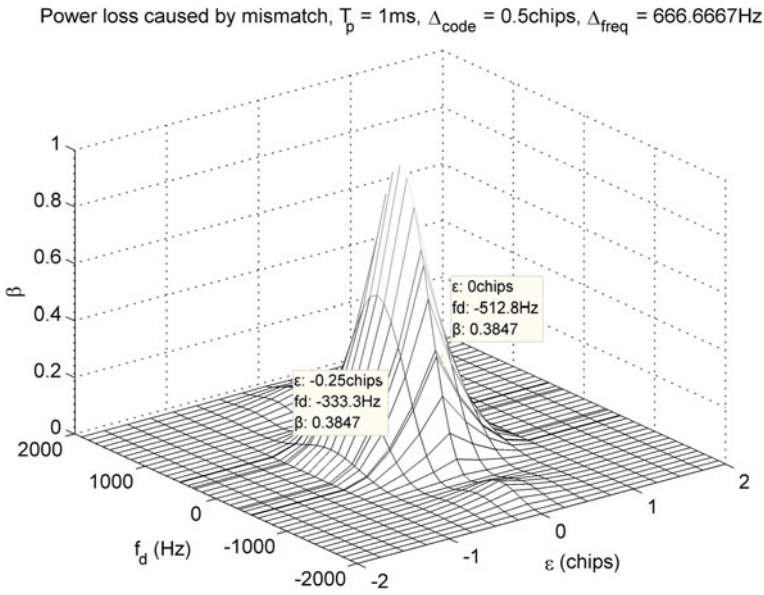

Fig. 49.1 Curve: β versus ε and f_d

Figure 49.2 gives the FLL discriminator curves of "four-quadrant" frequency discriminator $D_{FLL,4}$ and "dual-quadrant" frequency discriminator $D_{FLL,2}$ simultaneously.

$$D_{FLL\_4} = \frac{\text{atan2}(\text{Cross}, \text{Dot})}{2\pi T_p} \tag{49.2}$$

$$D_{FLL\_2} = \frac{1}{\sqrt{\text{Cross}^2 + \text{Dot}^2}} \frac{\text{Cross} \cdot \text{sgn}(\text{Dot})}{2\pi T_p} \tag{49.3}$$

where T_p is the predetection integration time, sign(.) denotes signum function, Cross and Dot are called as cross item and dot-product item respectively, with definition as

$$\text{Cross} = I_P(n-1)Q_P(n) - I_P(n)Q_P(n-1) \tag{49.4}$$

$$\text{Dot} = I_P(n-1)I_P(n) + Q_P(n-1)Q_P(n) \tag{49.5}$$

with I_P and Q_P being the in-phase and quadrature-phase correlation values respectively.

As shown in Fig. 49.2, giving $T_p = 1$ ms, the normal operation range of dual-quadrant discriminator $D_{FLL,2}$ is -250 to 250 Hz. If the absolute value of residual carrier Doppler frequency falls into the abnormal range of 250–750 Hz, then the FLL would false lock at ± 500 Hz [i.e., $1/(2T_p)$].

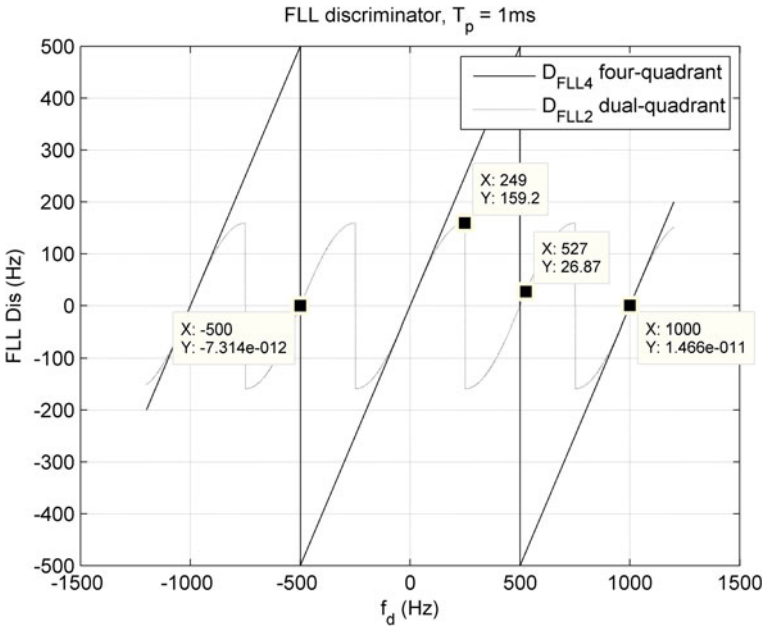

Fig. 49.2 FLL discriminator curve

Since the FLL and DLL work simultaneously, the last stabilized error pattern caused by FLL frequency false locked problem is <0 chips, ±500 Hz>, which has corresponding power loss of $\beta = 0.41$, larger than the acquisition threshold of $\beta = 0.38$, so the traditional Lose Loop Detector based on correlator power fading detection can NOT detect FLL frequency false lock phenomenon. Referring to [1], the PLL can NOT detect above anomaly too. Therefore, it is necessary to propose new methods to solve above problem.

49.3 Solutions

Referring to Sect. 49.1, a simple but application limited solution was first proposed by Li et al. [1], which could NOT work for the situations of only one or two PRN code periods existing in one information bit (such as GALILEO E1-B), or the situations of high rate secondary code being modulated (such as GPS L5, GALILEO E1-C, E5a, and E5b).

To overcome the shortcoming of [1], following two simple but universal solutions were proposed in this paper: A. Instead adopting the "four-quadrant" frequency discriminator; B. Inserting a novel frequency false lock detecting and correction mechanism between "dual-quadrant" FLL and Phase Lock Loop (PLL).

49.3.1 Solution A: Instead Adopting the "Four-Quadrant" Frequency Discriminator

Adopting the "four-quadrant" frequency discriminator can completely eliminate the FLL frequency false lock phenomenon.

Referring to Fig. 49.2, under the condition of four-quadrant discriminator $D_{FLL,4}$ being adopted, if the absolute value of residual carrier Doppler frequency larger than 500 Hz (e.g. 527 Hz), then the FLL would false lock at ±1,000 Hz, resulting in the correlator power fading to zeros. At that time, the traditional Lose Loop Detector based on correlator power fading detection will work and assert that tracking loops lose lock, and then the re-acquisition procedure would restart subsequently. After searching all the remaining PRN code phases, re-acquisition procedure would step into a new frequency (e.g., $527-627 = -100$ Hz) and continue to search the total PRN code phases until acquisition succeed. Since −100 Hz falls into the normal operation range of dual-quadrant discriminator $D_{FLL,4}$, the FLL will work normally. Therefore, the dual-quadrant discriminator can completely eliminate the FLL frequency false lock phenomenon, with the cost of acquisition time being obviously extended, which caused by an extra loop lose lock and re-acquisition procedure.

49.3.2 Solution B: Inserting a Novel Frequency False Lock Detecting and Correction Mechanism

Figure 49.3 gives the state flow of frequency false lock detecting and correction mechanism which is based on power judgment. After acquisition completion, "FLL State" is first executed. At FLL State, "dual-quadrant" frequency discrimination strategy is adopted, and the carrier frequency tends to lock at 0 or ±500 Hz. After A seconds, setting reference frequency (RefFreq) equal to the current frequency control word (FW), and then jumping into "Frequency False Lock Detecting and Correction State".

"Frequency False Lock Detecting and Correction State" consists of four substates with "Current Frequency Power Calculation State" being first executed. At that State, simply setting FW equal to RefFreq, and calculating the signal power of current frequency point (denotes as CurPower). After B seconds, it jumps into "+500 Hz Frequency Power Calculation State". At that State, simply setting FW equal to RefFreq plus 500 Hz, and calculating the signal power of current frequency point (denotes as PlusPower). After B seconds, it jumps into "−500 Hz Frequency Power Calculation State". At that State, simply setting FW equal to RefFreq minus 500 Hz, and calculating the signal power of current frequency point (denotes as MinusPower). After B seconds, it finally jumps into "False Lock Detecting and Correction State". At that State, finding the max value among

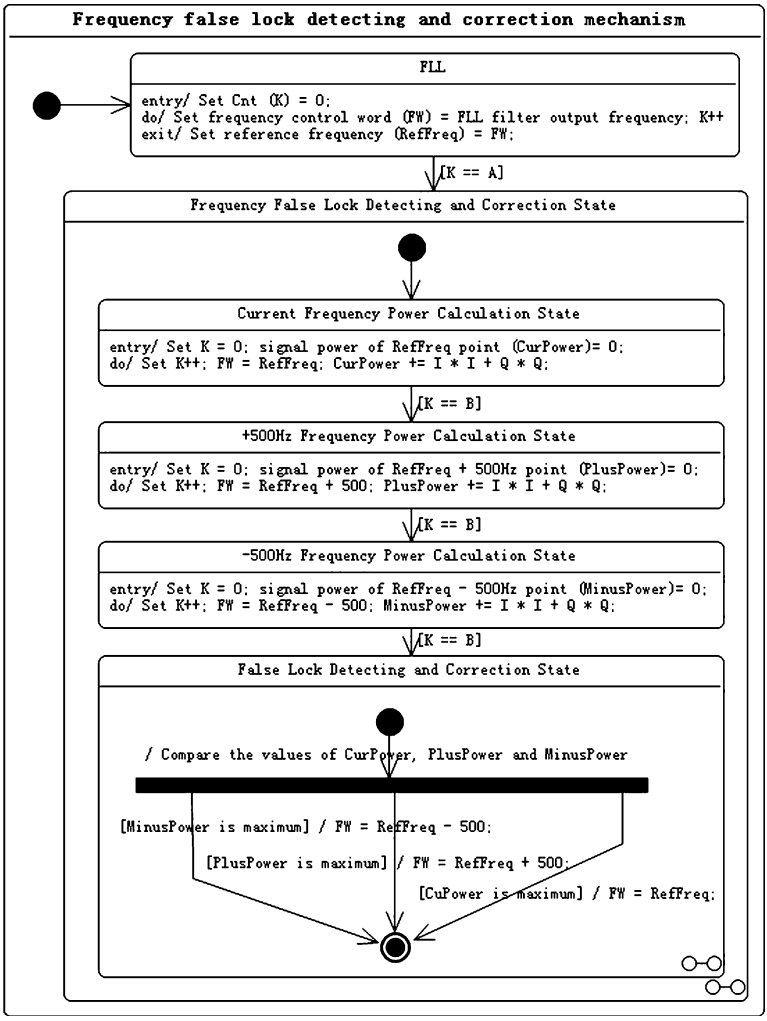

Fig. 49.3 State flow for frequency false lock detecting and correction algorithm

CurPower, PlusPower and MinusPower, and then setting FW equal to the right frequency corresponding to the maximum one.

Computer simulation was carried out to validate solution B. The simulation conditions are as follows: setting C/N_0 as 39 dB-Hz, the residual carrier Doppler frequency as 700 Hz, and the predetection integration time as 1 ms, which resulting the normal operation range of dual-quadrant discriminator being −250 to 250 Hz. Taking second-order FLL filter, with filter bandwidth as 12 Hz. Setting A equal to 2 s, B equal to 10 ms.

Figure 49.4 gives the Simulation result, with Fig. 49.4a being the global frequency tracking error curve, while Fig. 49.4b is the partial curve before frequency

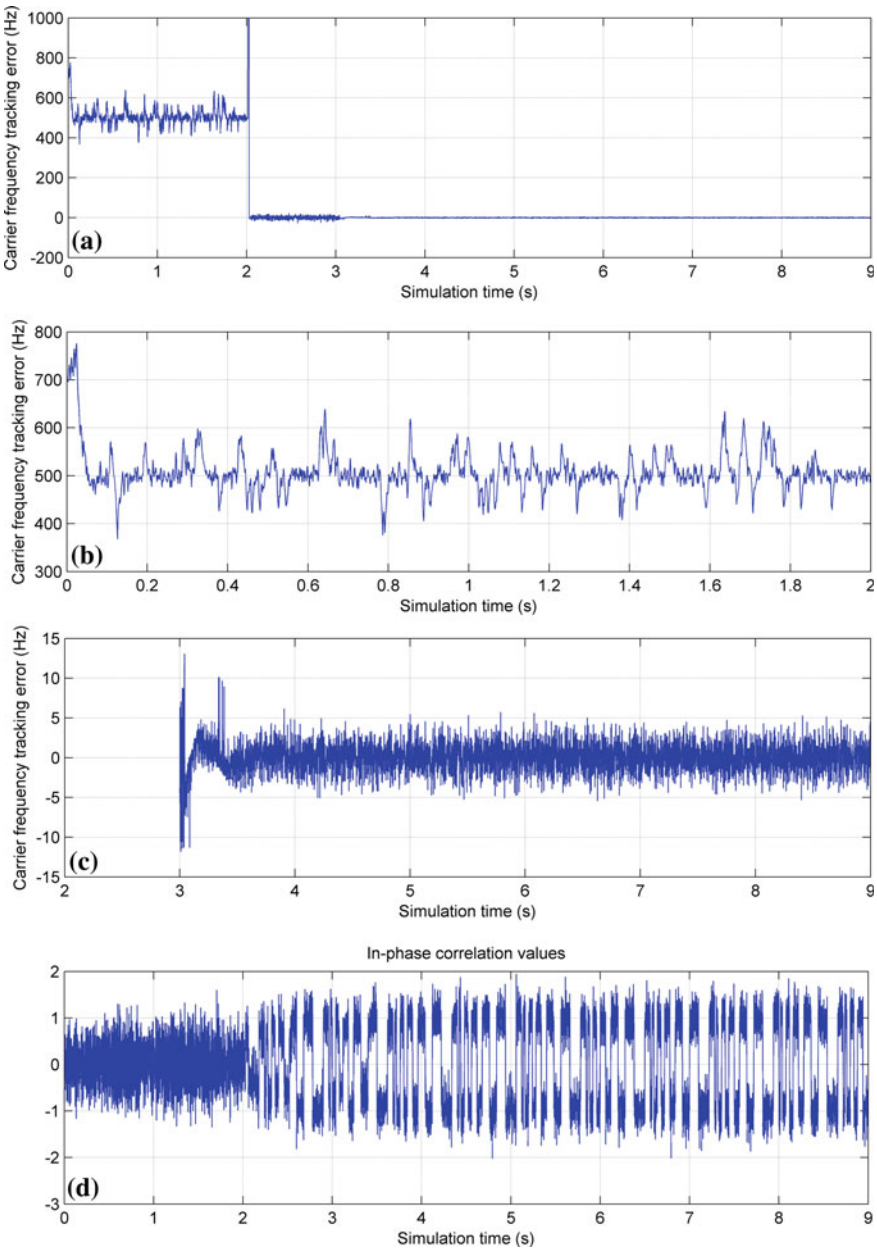

Fig. 49.4 Simulation for frequency false lock detecting and correction algorithm. **a** Carrier frequency tracking error (*global curve*). **b** Carrier frequency tracking error (*partial curve*, *before correction*). **c** Carrier frequency tracking error (*partial curve*, *after correction*). **d** In-phase correlation values

false lock correction, and Fig. 49.4c is the partial curve after the correction. Figure 49.4d is the in-phase correlation values. As shown in Fig. 49.4b, from 0 to 2 s, "dual-quadrant" frequency discriminator was adopted, and carrier frequency error was false locked from 700 to 500 Hz. As shown in Fig. 49.4a, from 2 to 2.03 s, frequency false lock detecting and correction mechanism was executed, and the carrier frequency error was corrected to 0 Hz around. As shown in Fig. 49.4c and d, from 3 to 9 s, FLL assist PLL frequency tracking algorithm was executed, and the carrier frequency error works normally with ±5 Hz jittering. At this time, bit synchronizes normally.

49.4 Conclusion

It was found that when sequentially adopting the "sliding correlation" acquisition strategy and the "dual-quadrant" frequency discrimination strategy, the FLL occasionally operates abnormally. The solutions found in literature have limitation that could NOT work for the situations of only one or two PRN code periods existing in one information bit, or the situations of high rate secondary code being modulated. To overcome above shortcomings, two simple but universal solutions were proposed in this paper: A. Instead adopting the "four-quadrant" frequency discriminator instead; B. Inserting a novel frequency false lock detecting and correction mechanism between "dual-quadrant" FLL and Phase Lock Loop (PLL). Theory analysis and simulation test show that the proposed solutions can effectively solve the FLL frequency false lock problem. The implementations are simple but universal, and they apply to all GNSS signal structures.

References

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